Power Mixed Signal ASIC Library

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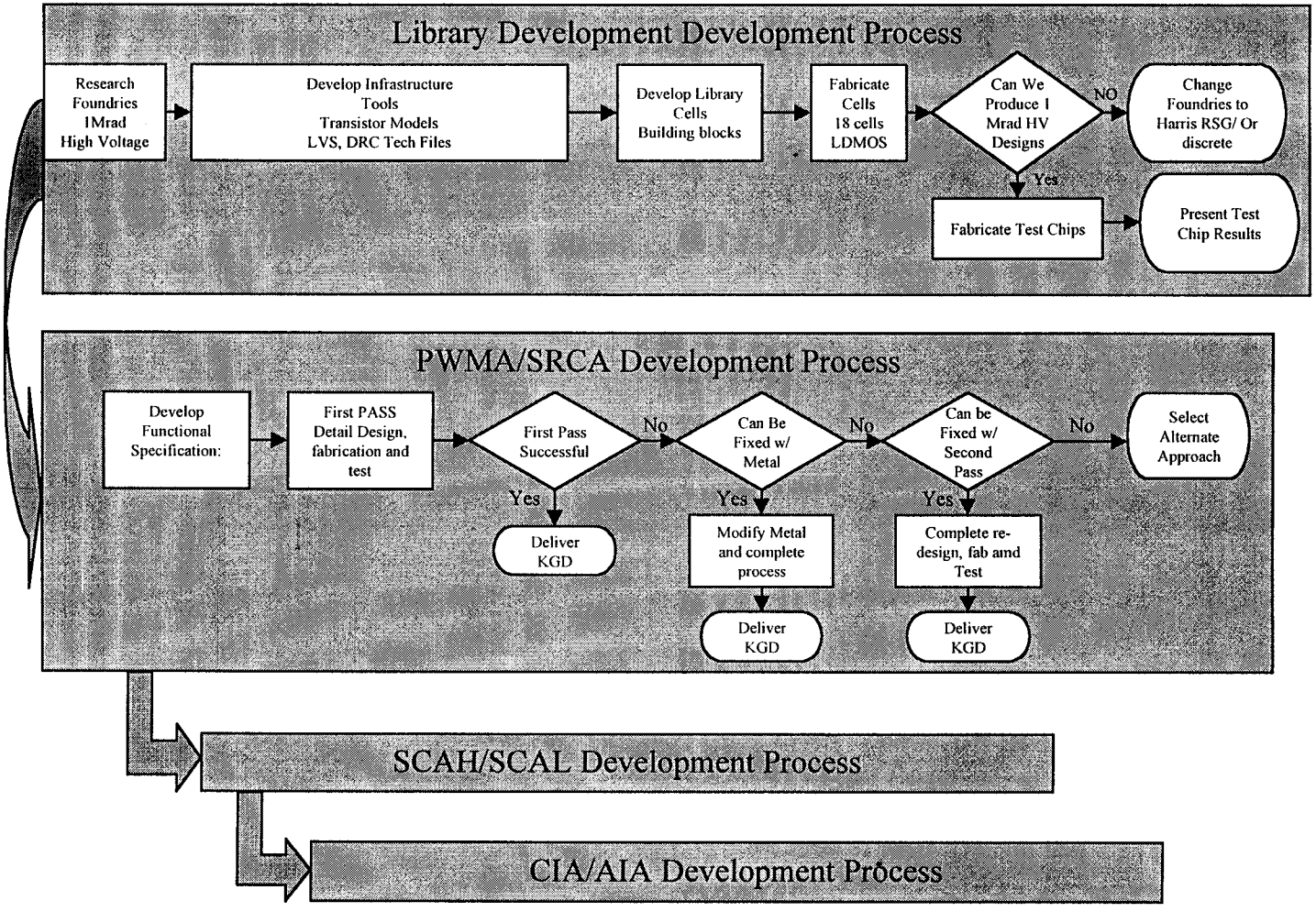
Rationale/Challenges

- Reduce mass, volume and power
- Survive severe environments
  - Europa radiation environment
  - Life
- High reliability
  - Power cross-strap and current limiting on chip
- Low voltage process
  - Needed to develop high voltage transistors
  - High common mode transients

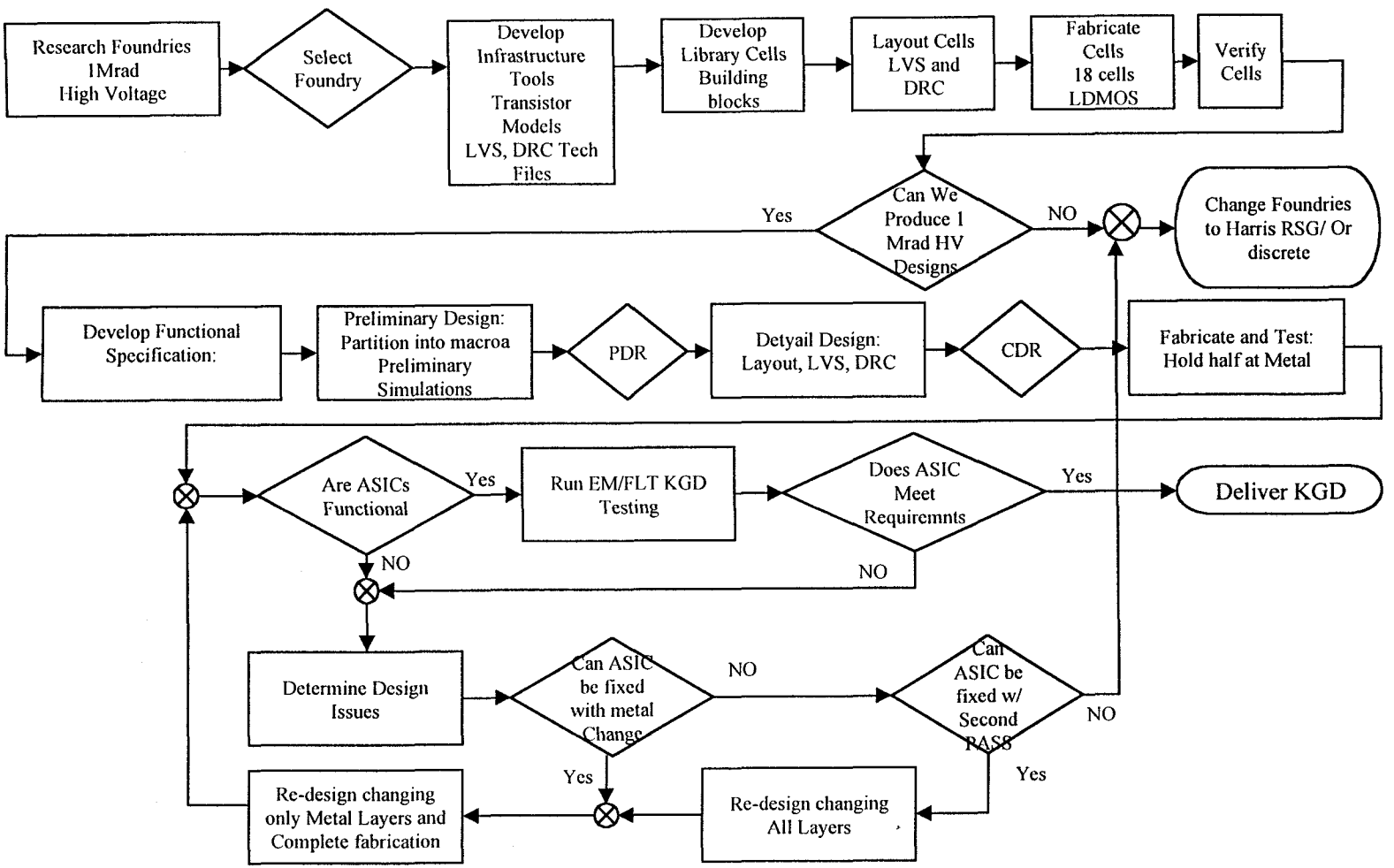
Boeing/JPL Cell Development

- Identify Need for a Function
- Develop Preliminary Spec
- Design the Cell So That Simulation Results Predict Success
- Plan for Test/Design In Test Points and Structures
- Review by Peers
- Perform Layout
- Integrate with Other Cells
- Release to Foundry
- Prepare for Test
- Develop Behavioral Model
- Perform Testing to Verify Performance to Specifications, Including Rad
- Update Spec and Behavioral Model as Required
- Freeze the Design
- Store Parts for Use in Breadboards

Power Mixed Signal ASIC Development Plan

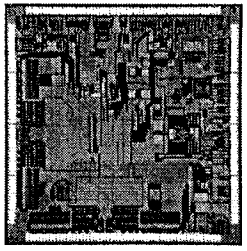


Mixed Signal ASIC Detail Design Flow

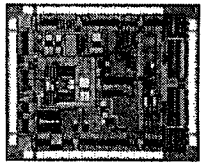


Europa Orbiter/X2000 Avionics Industry Briefing

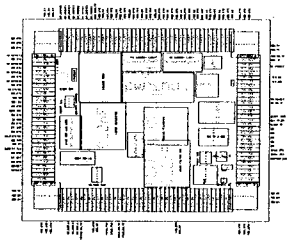
- **Pulse Width Modulator (PWMA)**
  - High frequency switching regulator (1 Mhz)
  - 2 A transient 1 Mhz CHFET driver
- **Synchronous Rectifier Controller SRCA**
  - High Speed Synchronous CHFET Driver
  - High Voltage Linear Regulator
- **Switch Control ASIC High Side (SCAH)**
  - Floating High speed linear MOSFET control
  - Low offset current sense
- **Switch Control ASIC Low Side (SCAL)**
  - Ground Referenced Power Switch Control
  - Charge Pump, Level Shifting (40V)
- **Command Interface ASIC (CIA)**
  - Microcontroller with imbedded RAM,ROM
  - A-to-D Converter, Power Cross-strap
- **Analog Interface ASIC (AIA)**
  - Isolated I2C Bus Interface



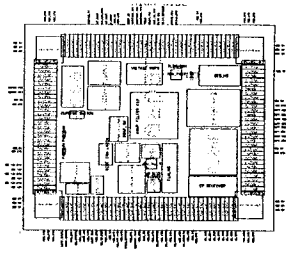
PWMA
HX2080



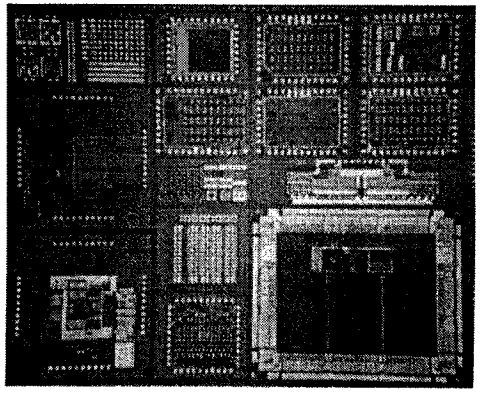
SRCA
HX2040



SCAH Layout
CDR: 6/28/01



SCAL Layout
CDR: 6/28/01



A/D Test CHIP

Status

- Boeing completed fabrication and test of the initial library
- Completed fabrication of two test chips
  - Boeing Library
  - A/D Test Chip
- Completed fabrication of the PWMA and SRCA first pass
  - In test, verifying functionality (>90%)
  - POR timing issue, Auto-zero offset
- SCA CDR is planned for 6/28/01
  - PSPICE behavioral models are complete
- CIA CDR is planned for 10/22/01